Interconnect Delay Compensation in Timing Analysis for Designs Containing Multiple Voltage Domains

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1. Introduction

A timing signal may flow from one voltage domain to another different voltage domain in a circuit that contains multiple voltage domains. When a cell drives its receiver cell with a different supply voltage, the measuring trip-points at the inputs of the receiver cell (usually 50% of V_{DD} for the interconnect delay and 20%-80% (or 10%-90%) of V_{DD} for the transition delay) could be different from those of the driving cell. A frequently used solution is to insert level shifters between two different voltage domains so that the circuit timing can work as desired. However, a robust timing analysis tool still needs to handle the situation and compensate the difference when level shifters are missing between different voltage domains. This paper presents a compensation technique that has been adopted in Incentia's TimeCraft™ static timing analyzer to properly model interconnect delay and transition under such a situation.

2. Compensation Method for Voltage Difference

Assume that a cell is driving an interconnect network, as shown in Figure 1, and its supply voltage is V_{DD}.

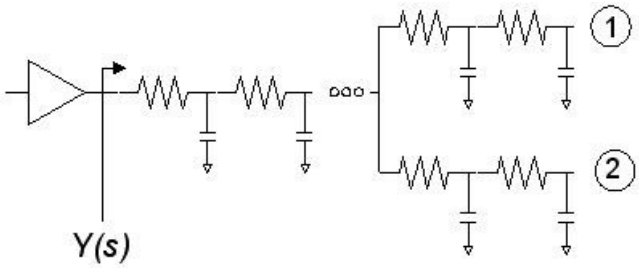

Figure 1: Interconnect network example

We can analyze the output waveform of each receiver point at ① & ②, by taking the convolution integral with the impulse response. Since the waveform equation at the receiver point can be obtained, we can measure the upper / lower thresholds (20%-80% or 10%-90%) of the transition delays exactly by Newton-Raphson iteration.

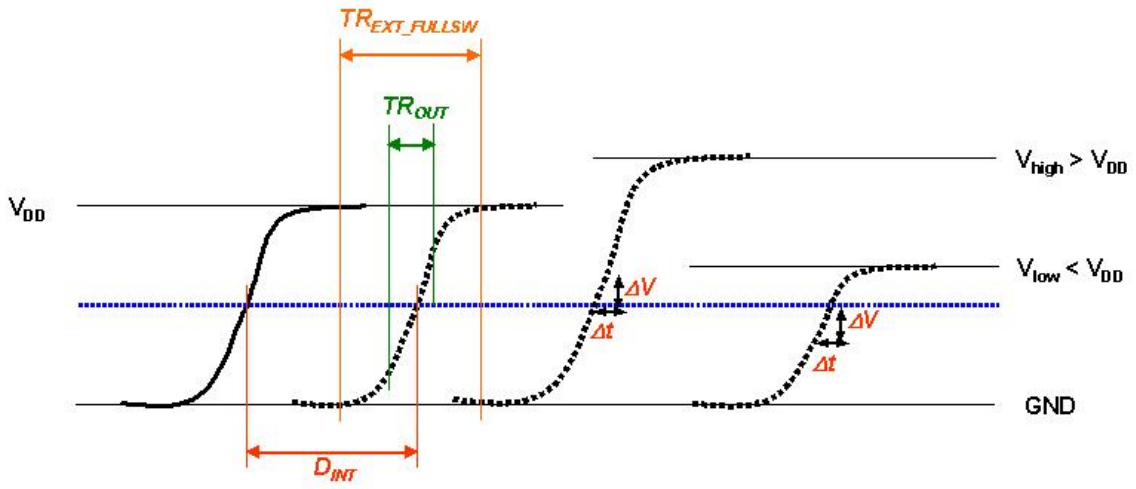

Figure 2: Waveforms at driving point and receiver points

The supply voltage from driving cell is V_{DD}. Thus, the waveform at the receiver point has the same voltage swing from GND to V_{DD}. When the receiver cell has a different supply voltage, such as V_{high} or V_{low}, as shown in Figure 2, the interconnect delay is compensated by estimating Δt in Figure 2.

First, we obtain the measured output transition delay, TR_{OUT} as shown in Figure 2. Then, we extend the transition delay by dividing it with the trip-point reference (*UpperTh* & *LowerTh* from the Liberty).

$$TR_{EXT\_FULLSW} = \frac{TR_{OUT}}{(UpperTh - LowerTh)} \quad (1)$$

TR_{EXT_FULLSW} is the time consumed for the output waveform to take a full swing from GND to V_{DD}. To estimate Δt, it is necessary to calculate the voltage difference, ΔV, by considering the input threshold trip-point (usually 50%).

$$\Delta V = \left(DelayTh_{receiver} \times V_{high}\right) - \left(DelayTh_{driver} \times V_{DD}\right)$$
$$or \qquad (2)$$
$$= \left(DelayTh_{receiver} \times V_{low}\right) - \left(DelayTh_{driver} \times V_{DD}\right)$$

Since TR_{EXT_FULLSW} is the time for full swing from GND to V_{DD}, we can estimate the time difference for voltage difference, ΔV, by

$$\frac{\Delta t}{TR_{EXT\_FULLSW}} = \frac{\Delta V}{V_{DD}}$$
$$\therefore \Delta t = \frac{TR_{EXT\_FULLSW} \times \Delta V}{V_{DD}} \qquad (3)$$

Substituting Eqn (1) & (2) into Eqn (3) gives the compensation equation, as follows.

$$\Delta t = \frac{TR_{OUT}}{(UpperTh - LowerTh)} \times \frac{\left(DelayTh_{receiver} \times V_{high} - DelayTh_{driver} \times V_{DD}\right)}{V_{DD}}$$
$$or \qquad (4)$$
$$= \frac{TR_{OUT}}{(UpperTh - LowerTh)} \times \frac{\left(DelayTh_{receiver} \times V_{low} - DelayTh_{driver} \times V_{DD}\right)}{V_{DD}}$$

In case of rising transition, this time difference is added to the measured interconnect delay under V_{DD}. On the other hand, in case of falling transition, this time difference is subtracted from the measured interconnect delay.

For the output transition delay compensation, we multiply the ratio of the receiver supply voltage over the driver supply voltage to the measured output transition delay.

$$TR_{COMPENSATED} = TR_{OUT} \times \left(\frac{V_{high}}{V_{DD}}\right)$$
$$or \qquad (6)$$
$$= TR_{OUT} \times \left(\frac{V_{low}}{V_{DD}}\right)$$

3. Consideration of Level Shifter

When a driver or receiver cell is a level shifter, we do not need to compensate the delay difference. A level shifter is a cell that has a level-shifter attribute defined in the *cell* section of a Liberty file. The level shifter is designed to bridge signals between two different supply voltage domains, and is already characterized with respect to its different input and output supply voltages. Thus, no compensation is needed.

4. Other Compensations

Two additional compensations are also considered.

- Slew derate difference
  If the driver and receiver cells have different slew derates for upper / lower thresholds, we should also consider compensation. This is always considered, regardless of supply voltage difference, for transition delay compensation.

- Upper / lower threshold difference
  This upper / lower threshold difference is only applied when wire-load model is used for this net. When RC interconnect network is annotated to the net, we measure the upper / lower thresholds exactly from the output waveform equation. Thus, it is automatically considered.

Refer to Section 5 to see when these compensations are applied.

5. Parameter to Control Compensation

Compensation due to the supply voltage difference is based on the assumption that the interconnect delay should be measured at the threshold point of the receiver's supply voltage reference. For example, assume that the driver cell is in 1.2V voltage domain, and the receiver cell is in 0.9V voltage domain. When the driver is taking the rising transition, the interconnect delay should be measured between the time points of 0.6V (50% of 1.2V) and 0.45V (50% of 0.9 V). Since 0.45V can come first, it requires compensation. In timing analysis, we can address this issue by using automatic compensation. However, this may be a design problem since a level shifter is needed from design point of view.

Furthermore, consider that a cell is driving the interconnect network again in Figure 1. Since the driver cell has V_{DD} as the supply voltage, the output response at each receiver point has V_{DD} voltage swing too. If the driver cell is in 0.9V voltage domain and the

receiver is in 1.2V voltage domain, we have to measure 0.24V (20% as lower threshold) and 0.96V (80% as upper threshold) for the transition delay. But the supply voltage of the driver cell is 0.9V, and thus, the output waveform never reaches 0.96V at the receiver point. Although the compensation can be done in timing analysis, it is not done correctly.

In the early design stage, you may want to quickly get the preliminary timing analysis result of the design without fixing the problem caused by signals crossing different voltage domains. In this case, automatic compensation can be used. On the other hand, in the later design stage when place and route are done, you should make sure level shifters are inserted correctly whenever signals are crossing different voltage domains. Automatic compensation should not be applied. And signals crossing different voltage domains without proper level shifters in place should be detected and fixed at this stage. Therefore, a parameter is introduced to turn on / off the automatic compensation.

The following table summarizes what compensations, including voltage, slew derate, and upper/lower threshold, are considered together with the parameter setting in each case. When proper level shifters are in place, no voltage compensation will be done when crossing different voltage domains no matter you turn on this parameter or not. In the early design stage, usually wire load model is used for timing analysis. We suggest you turn on the automatic compensation because level shifters between different voltage domains may not be inserted at this time. In the later design stage, detailed RC information is available and back annotated to timing analysis. At this stage, you should turn off the automatic voltage compensation so that any remaining design problems caused by voltage differences can be observed.

When RC is annotated	Level Shifter	without Level Shifter		with Level Shifter	
	parameter	true	false	true	false
	delay	ΔV	-	-	-
	transition	ΔV ΔSlewDerate	ΔSlewDerate	ΔSlewDerate	ΔSlewDerate
When WLM is used	Level Shifter	without Level Shifter		with Level Shifter	
	parameter	true	false	true	false
	delay	ΔV	-	-	-
	transition	ΔV ΔSlewDerate Δupper/lowerTh	ΔSlewDerate Δupper/lowerTh	ΔSlewDerate Δupper/lowerTh	ΔSlewDerate Δupper/lowerTh

6. Incentia Timing Analysis Products

Incentia offers static timing analysis (STA), signal integrity analysis, and statistical STA through its TimeCraft product line. TimeCraft is a full-chip, gate-level static timing analyzer for timing sign-off. It is the fastest STA available in the market and has been proven through numerous customer tape-outs. TimeCraft has demonstrated unparalleled advantages in runtime and capacity that dramatically reduce total timing verification turnaround time.

TimeCraft's built-in delay calculator takes in parasitic RC information through SPEF back annotation file, and libraries in NLDM, CCS, or ECSM format. It generates accurate timing analysis results, within 2% of SPICE results in general. It also has special algorithms to handle extreme cases, such as long wires, long wires with fat metals, high fan-out nets, mesh RC networks, parallel buffers, and cross-linked non-tree clock networks. TimeCraft performs automatic interconnect delay compensation when crossing different voltage domains as described in this paper.